Speed Control of DC Motor Using Phase-Locked Loop

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Abstract

The purpose of controlling the speed of dc motors can be accomplished by various methods. 'Phase-locked loop control' is one of the most convenient and efficient methods for the same. The Phase-locked loop principle has been used in applications such as FM (frequency modulation), stereo decoders, frequency synthesized transmitters and receivers, FM demodulators and frequency shift keying (FSK) decoders. This paper explains the phase-locked loop based speed control of a dc motor.

Contents

1. Introduction

The speed of a d.c.motor can be controlled by mainly two ways:

- Electrical speed control
- Electronic speed control

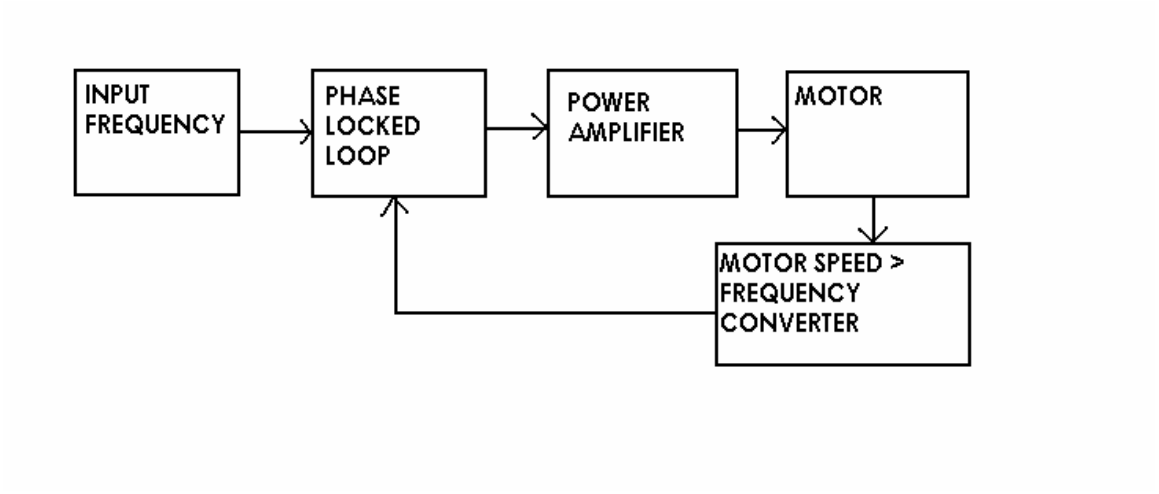
Electrical speed control can be achieved by following methods:

- Variation of Flux or Flux Control Method
- Armature or Rheostatic Control Method
- Voltage Control Method

Electronic speed control can be achieved by following methods:

- Thyristor speed control
- Chopper control
- By using Phase-locked loop

2. System model

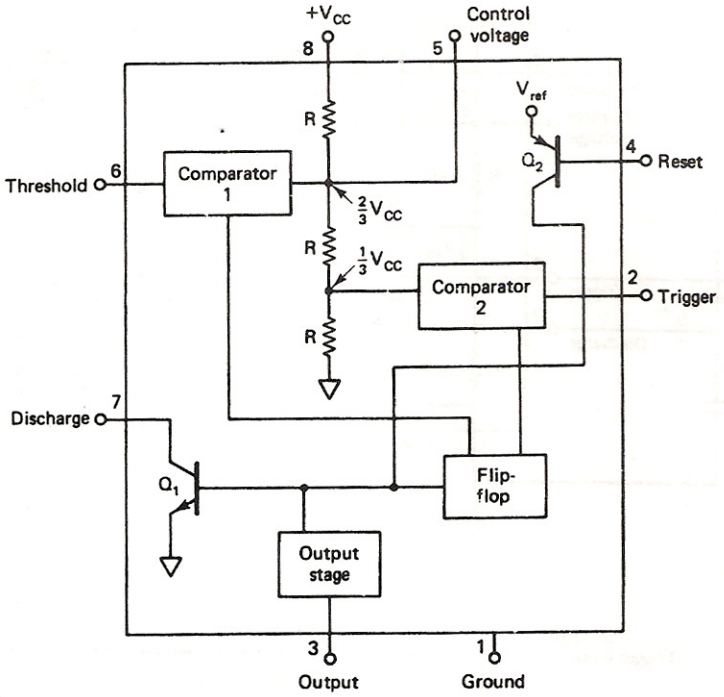


[Figure 1: Basic blocks of the model]

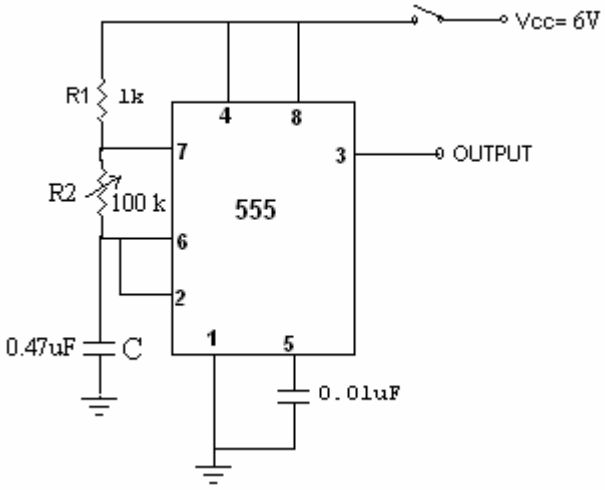
- The entire system of PLL control consists of five blocks as shown in the figure1. The input frequency decides that at what constant speed, the motor should be run. This frequency is generated by a function generator (Note: Here 555 timer's astable operation is used for getting the desired frequency).
- This input frequency is given to the phase locked loop IC (LM565). When the load on the motor fluctuates, according to that, the speed of the motor varies. The 'motor speed => frequency converter' converts the speed of motor into proportional frequency and sends it to the phase locked loop. (Note: This frequency is termed as the output frequency.)
- The phase detector of the phase-locked loop compares the input and output frequencies and generates a dc output voltage, which is proportional to the phase-difference between the two frequencies.
- A power amplifier amplifies this dc voltage and then, it is given to the motor, so the motor gets the desired speed.

2.1 Input Frequency

- The input frequency is generated by a function generator. Here, the astable operation of a 555 timer is used to get the desired input frequency.



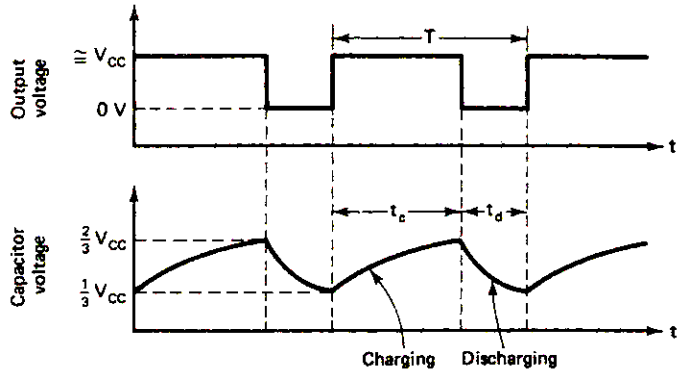
[Figure 2: Block diagram of 555]



[Figure 3: Astable operation of 555]

- Figure3 shows the 555 timer connected as an astable multivibrator. Initially, when the output is high, capacitor C starts charging toward Vcc through R1 and R2. As soon as the voltage across the capacitor equals 2/3 Vcc, comparator 1 triggers the flip-flop, the output switches low (Refer figure2).

- Now capacitor starts discharging through R2 and transistor Q1. When the voltage across C equals 1/3 Vcc, comparator 2's output triggers the flip-flop, and the output goes high. Then the cycle repeats. The output voltage and capacitor voltage waveforms are as shown in the figure4.



[Figure 4: Output voltage and capacitor voltage waveforms]

- As shown in the figure4, the capacitor is periodically charged and discharged between 2/3 Vcc and 1/3 Vcc, respectively. The time during which the capacitor charges from 1/3 Vcc to 2/3 Vcc is equal to the time the output is high and is given by

$$Tc = 0.69(R1+R2)\ C \quad \text{(2.1a)}$$

- Similarly, the time during which the capacitor discharges from 2/3 Vcc to 1/3 Vcc is equal to the time the output is low and is given by

$$Td = 0.69(R2)C \quad \text{(2.2b)}$$

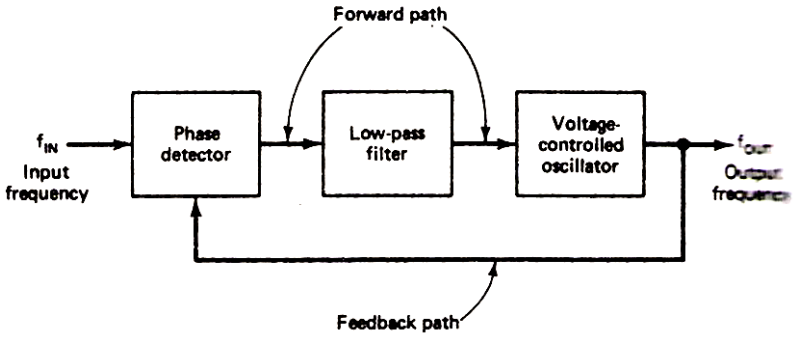
- Thus the total period of the output waveform is

$$T = Tc + Td = 0.69(R1+2R2)\ C \quad \text{(2.3c)}$$

- This gives the frequency of oscillation as

$$f = 1 / T = 1.45/((R1+2R2)\ C) \quad \text{(2.4d)}$$

2.2 Phase-Locked Loop

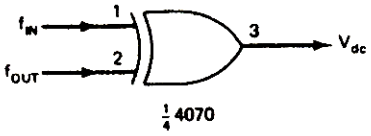


[Figure 5: Idea of working of a phase-locked loop]

- Figure5 shows the PLL in its basic form. The phase detector is a device that compares two frequencies, generating an output that is a measure of their phase difference (if, for example, they differ in frequency, it gives a periodic output at the difference frequency).
- If fin doesn't equal fvco, the phase-error signal, after being filtered and amplified, causes the VCO frequency to deviate in the direction of fin . If conditions are right, the VCO will quickly "lock" to fin, maintaining a fixed relationship with the input signal. At that point the filtered output of the phase detector is a dc signal, and the control input to the VCO is a measure of the input Frequency.
- Since the VCO output can be a triangle wave, sine wave, or whatever, this provides a nice method of generating a sine wave, say, locked to a train of pulses. In short, PLL goes through three states : Free running, Capture and Phase-locked.

2.2.1 Phase Detector

- If two signals are fed into a phase detector, being equal in phase and frequency, there will be no output from the detector.
- However, if these signals are not in phase and frequency, the difference is converted to a DC output signal. The greater the frequency/phase difference in the two signals, the larger the output voltage.
- Depending on whether the analog or digital phase-detector is used, the PLL is called either an analog or digital type, respectively. Examples of digital phase-detectors are:
  - Exclusive-or phase detector
  - Edge-triggered phase detector
  - Monolithic phase detector

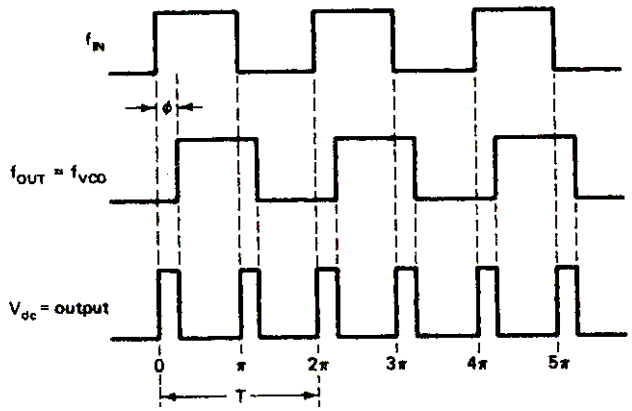


Truth table

Inputs		Outputs
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

L = Low
H = High

[Figure 6: Exclusive-OR gate]



[Figure 7: Input and output waveforms]

- The output of the exclusive-or gate is high only when fin or fout is high as shown in the figure7. In this figure, fin is leading fout by 'phi' ($\varnothing$) degrees. The dc output voltage of the exclusive-or phase-detector is a function of the phase difference between its two inputs.

2.2.2 Low-pass Filter

- The function of the low-pass filter is to remove the high frequency components in the output of the phase-detector and to remove high frequency noise. More important, the low-pass filter controls the dynamic characteristics of the PLL. These characteristics include capture and lock ranges, bandwidth and transient response.
- The lock range is defined as the range of frequencies over which the PLL system follows the changes in the input frequency fin. On the other hand, the capture range is the frequency range in which the PLL acquires phase lock. Obviously, the capture range is always smaller than the lock range.

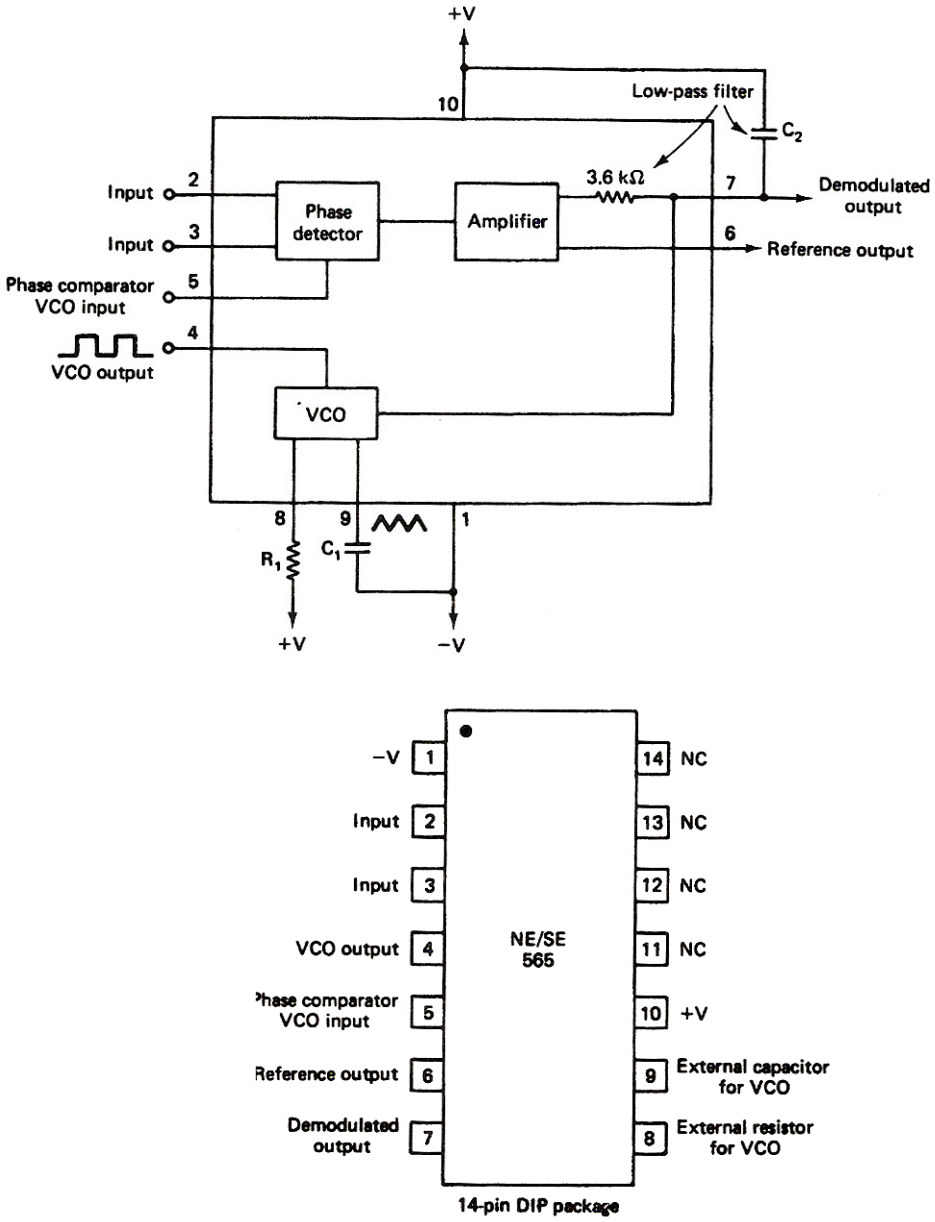
2.2.3 Voltage Controlled Oscillator

- The VCO generates an output frequency that is directly proportional to its input voltage.

2.2.4 Important electrical characteristics of LM565

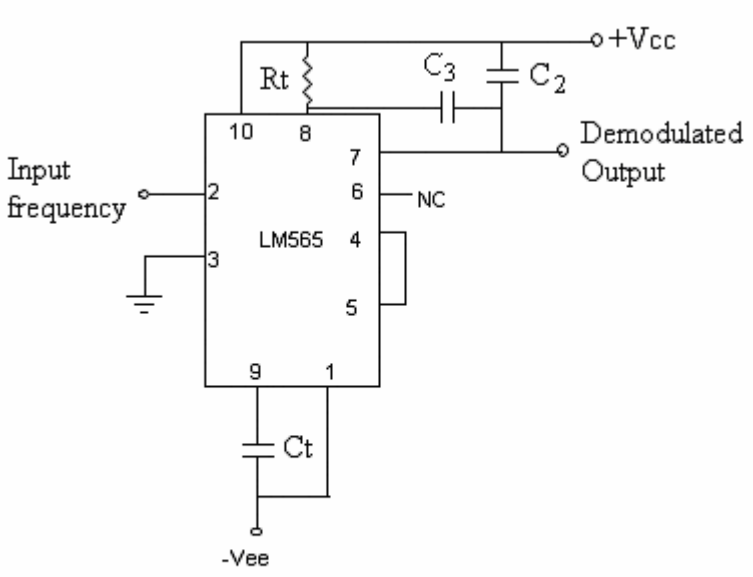
- Operating frequency range: 0.001 Hz to 500 kHz
- Operating voltage range: ±6 to ±12 V
- Input level required for tracking: 10mV rms minimum to 3V peak-to-peak maximum
- Input impedance: 10kΩ typically
- Output sink current: 1 mA typically
- Output source current: 10 mA typically
- Drift in VCO center frequency with temperature: 300 ppm/℃
- Drift in VCO center frequency with supply voltage: 1.5 %/V maximum
- Triangular wave amplitude: 2.4 V pp at ±6 V
- Square wave amplitude: 5.4 V pp at ±6 V
- Bandwidth adjustment range: <±1% to >±60%

2.2.5 Block Diagram of PLL

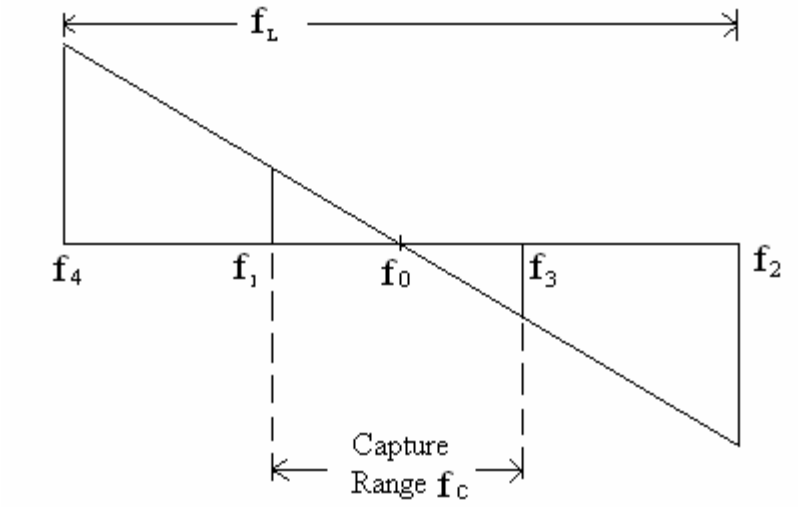


[Figure 8: Block diagram and pin diagram of phase locked loop]

2.2.6 Designing components of PLL



[Figure 9: General Circuit of PLL]



[Figure 10: Locking and Capture ranges of PLL]

Here,

f_o = Free-running Frequency of VCO

$$f_o = 1.2 / (4RtCt) \quad (2.2.6a)$$

f_L = Lock range

Where Rt and Ct are external resistor and a capacitor connected to pins 8 and 9, respectively.

- The VCO free-running frequency fout is adjusted externally with Rt and Ct to be at the center of the input frequency range. Although Ct can be any value, Rt must have a value between 2 kΩ and 20 kΩ. A capacitor CL connected between pin 7 and the positive supply (pin 10) forms a first-order low-pass filter with an internal resistance of 3.6 kΩ.
- The filter capacitor CL should be large enough to eliminate variations in the demodulated output voltage at pin 7 in order to stabilize the VCO frequency.
- The lock range fL and capture range fC of the PLL are given by the following equations:

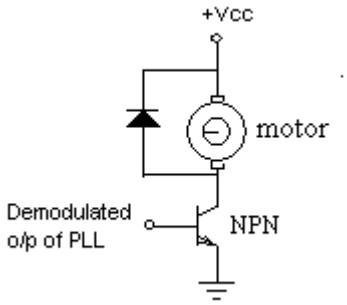
$$f_L = \pm (8\ fo / V)\ Hz \quad \text{(2.2.6b)}$$

Where V is (+V)-(-V)(volts)

$$f_C = \pm \left[\frac{f_L}{(2\pi)(3600)(C_2)} \right]^{1/2} \quad \text{(2.2.6c)}$$

- The lock range usually increases with an increase in input voltage but decreases with an increase in supply voltage.

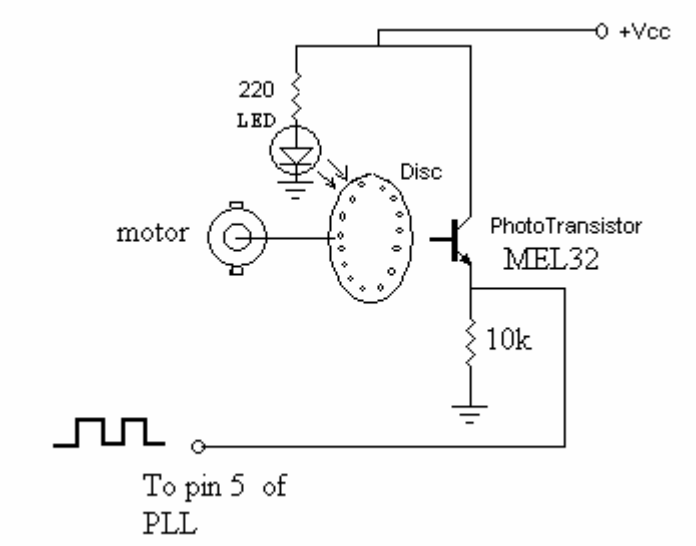
2.3 Power Amplifier and motor



[Figure 11: Power Amplifier Circuit]

- The demodulated output at pin 7 of PLL is fed into the base terminal of an NPN transistor. Thus the transistor performs switching action whenever its base voltage level is high. So the motor circuit gets completed and the motor runs at the desired speed.
- Free Wiley diode has been connected across the motor in order to protect it. It blocks the reverse directional current.

2.4 Motor Speed to frequency Converter

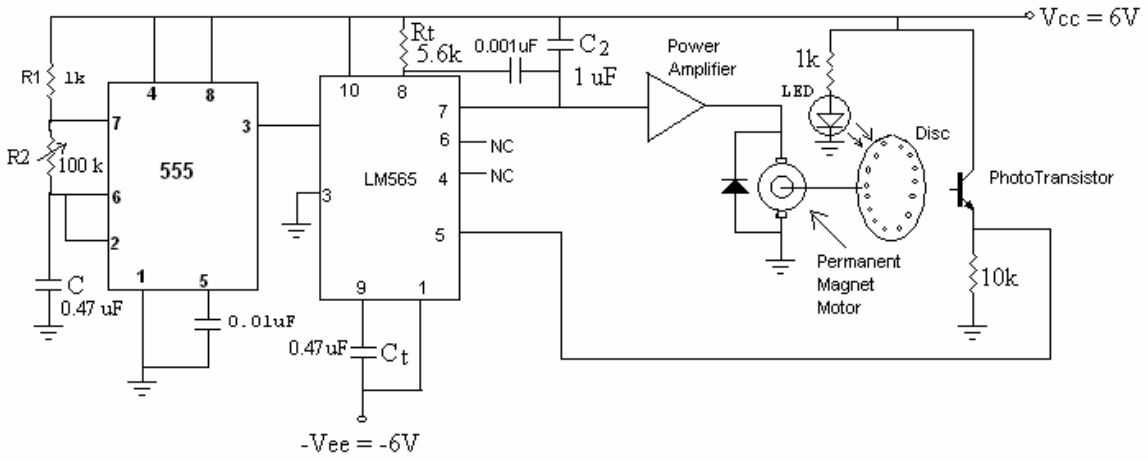


[Figure 12: Speed to Frequency Converter]

- As shown in the figure12, a circular disc of proper diameter and having uniformly distributed holes (or slots) on its periphery is mounted on the shaft of the motor.
- At one side of the disc, a Light Emitting Diode and on the other side a phototransistor is placed. The arrangement is such that the LED, holes of the disc and phototransistor are aligned in a straight line.
- When the obstacle appears between the LED and phototransistor, the phototransistor will not conduct. When the hole is placed between the LED and phototransistor, the phototransistor will conduct.
- This cycle repeats and hence a square wave is produced, the frequency of which is proportional to the speed of the motor. This frequency is termed as the output frequency and is fed back to the pin 5 of PLL.

2.5 Model Diagram

- The entire circuit model is represented in Figure13.



[Figure 13: Circuit Diagram for the Model]

Conclusion

- Whenever the load on the motor fluctuates, the difference between the input frequency and output frequency varies accordingly, which develops a dc error signal proportional to the phase-difference, due to which the voltage level at the pin 7 of PLL varies in order to get the predetermined constant speed of the motor. In this way, the speed control of dc motor can be achieved by using phase-locked loop.

References

- Ramakant A. Gayakwad, 'Op-Amps and Linear Integrated Circuits', Prentice Hall (Pearson Education), New Jersey
- http://www.alldatasheet.com/view.jsp?Searchword=LM5 (For data sheet of phase locked loop)

http://www.alldatasheet.com/view.jsp?Searchword=D55 (For data sheet of 555)